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Dual Line Sensor (DLS)
Vision Sensor Chip Description

GENERAL DESCRIPTION

The DLS Vision Sensor is an optical CMOS Dynamic Vision Sensor (DVS) chip that contains two lines of 256 pixels. Each pixel reacts to relative light intensity changes with low latency and ultra high time resolution, irrespective of absolute background illumination.

Unlike conventional image sensors the chip has no pixel readout clock but signals the detected changes instantaneously. This information is signalled as so-called "events" that contain the information of the responding pixels x-y addresses (address-event) in the imager array and the associated timestamp via a synchronous timed address-event-representation (TAER) interface. The sensor can produce two types of events for each pixel: "On"-events for a relative increase in light intensity and "Off"-events for a relative decrease (see diagram on next page).

Because the pixels of the vision sensor individually control their gain the sensor has a very high intra scene dynamic -> 120 dB.

As of these features the output of the sensor is not a conventional image but an abstract representation of the shape of moving objects in the scene, where the background is automatically suppressed.

Due to the on-chip pre-processing of the visual information the processing of the data is computationally less demanding as in image processing and the technology allows for especially compact "single-box" solutions.

SPECIFICATIONS

▶ Pixel resolution:	2 x 256
▶ Pixel pitch:	15 µm
▶ Photo diode area:	12 x 22.5 µm²
▶ Line separation:	250 µm
▶ Digital time stamp resolution:	100 ns
▶ Accuracy: (@1 kLux, 30% contrast)	0.2 µs [1]
▶ Latency: (@1 kLux, 30% contrast)	5 µs [1]
▶ Time resolution: (@4 kLux, 100% contrast)	5 µs [1]
▶ Sensitivity, min. pulse width: (@0.7 µW/pixel, ∞ contrast)	250 ns
▶ Sensitivity, min. contrast: (@1 kLux)	20%
▶ Dynamic range: (@21°C)	120 dB
▶ Data interface (TAE):	17 bit parallel
▶ Max. data rate:	20 Mevent/s
▶ Digital Configuration interface:	20 bit parallel
▶ Clock:	up to 40 Mhz
▶ Analogue bias inputs:	11
▶ CMOS technology:	0.35 µm
▶ Supply voltage:	3.3 V
▶ Power consumption, typ.:	250 mW
▶ Chip size:	3.6 x 5.2 mm
▶ Chip package type:	PGA 101
▶ Pin count:	100
▶ Operation temperature range:	0..55 °C
▶ Chip cover:	Glass Lid

ADVANTAGES

- ▶ Extremely high time resolution
- ▶ Wide intra scene dynamic range
- ▶ Data reduction 1-3(typ.) orders of magnitude compared to conventional line image sensors

[1] Single pixel data. Performance can degrade under high scene activity conditions due to shared TAER bus

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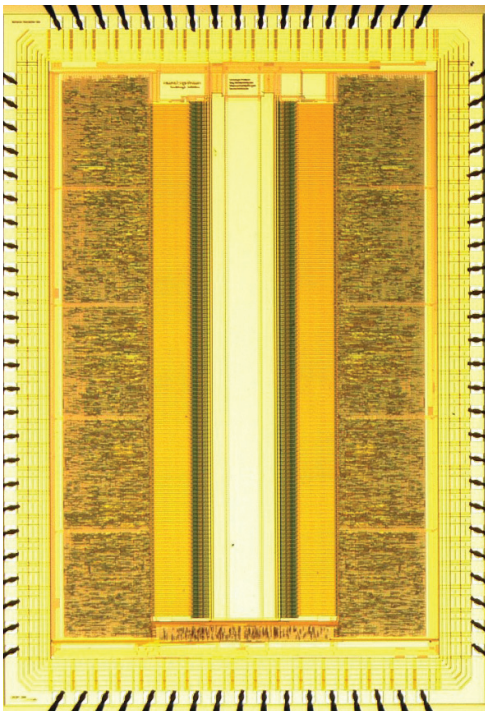
APPLICATIONS

- Industrial automation control systems
- Quality control systems
- High speed object tracking
- High speed shape detection, object counting and classification
- Real-time control systems
- Compact smart camera solutions



OPERATION PARAMETERS

The following operation parameters of the chip can be configured via the digital configuration interface:

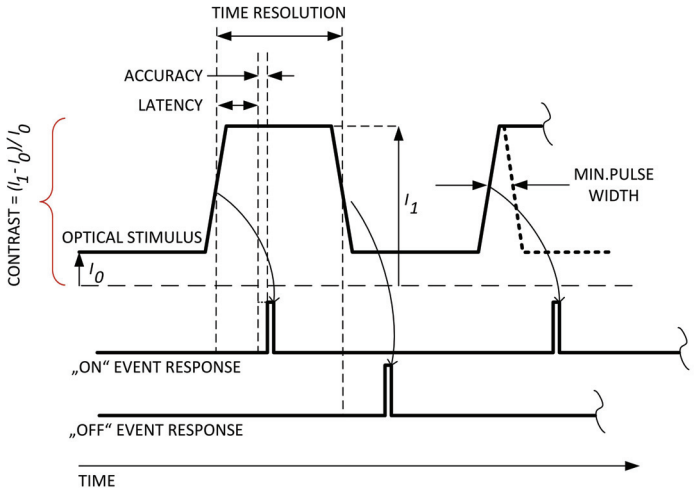
- Time stamp resolution
- Pixel masking
- Built in logic test

Analogue inputs are used to setup the following operation parameters:

- Contrast sensitivity
- Photoreceptor bandwidth
- Event rate limitation per pixel

EXPLANATION OF KEY PARAMETERS

The key parameters of the DLS pixel are depicted in the schematics below.



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